

SATA-Xactor Test Environment

Your Proven Path to SATA, AHCI, PATA Compliance Validation

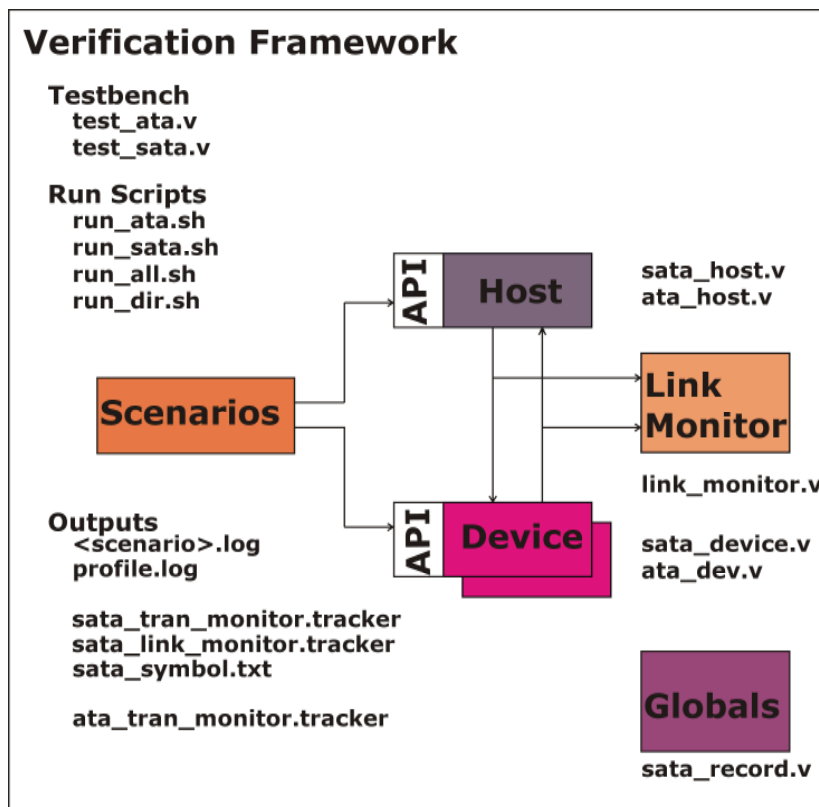


HIGHLIGHTS

- Complete solution to verify SATA 1/2/3, AHCI 1.2, ATA/ATAPI-8 components and peripherals
- Comprehensive BFM support – Host and Device models
- Testbench frameworks ease integration of DUV and running compliance testsuites
- Supports active test generation and passive link monitoring for easy integration in to any environment
- Comes with robust compliance test suites
- Supports all environments - Verilog, SystemVerilog, Specman, Vera, SystemC, C/C++, and VHDL
- Over 500 protocol checkers verify compliance and reports violations
- Functional coverage monitor reports device and command utilization

OVERVIEW

The SATA-Xactor test environment is a set of behavioral models (BFMs) and test suites that simulate the behavior of the ATA, SATA, and AHCI components. The models, provided in Verilog model format, are tools for system designers to exercise and debug the design of components/systems based on the various ATA standards. Designs under verification (DUVs) can be verified against all realistic system topologies including host or device topologies. The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. The test environment provides a high-level test API to interact with the behavioral models supporting hosts and devices, and a link monitor which passively monitors and reports ATA, SATA protocol violations, validates end-to-end transactions, and measures and reports transaction trace analysis of devices by sector address, bytes transferred, and command types utilized. In addition, the test environment includes a full suite of compliance test scenarios that verify hosts or devices comply fully with specifications.



PROGRAMMING INTERFACE

The SATA-Xactor test environment supports a powerful transaction API for the development of diagnostic test programs and is written in native Verilog and SystemVerilog HDLs. SystemC, Specman, Vera, VHDL, and C/C++ are supported through thin-client call layers. This simple, well-defined test API enables application designers to create any combination of transaction scenarios. From a single diagnostic test program, verification engineers can control multiple BFMs, direct normal and error transactions.

VERIFICATION FRAMEWORKS

The SATA-Xactor BFMs support ATA, SATA, and AHCI specifications. Several complete frameworks come configured to instantiate multiple BFMs including Host, Device, and Link Monitor. DUV integration and device configuration is simplified through normal power-on and reset sequences. Compliance tests can be easily run on pre-configured testbench for rapid evaluation of DUV in the framework. Compliance tests can be reused by all of ATA, SATA host or device configurations without modifications. Protocol checkers report assertion violations and trigger coverage. Verification test writers have the ability to selectively randomize 100s of device behaviors within the model for optimal test coverage under realistic conditions.

BFMs

The models support all ATA commands including Command Register and PACKET-based execution, command queuing, and other advanced ATA command processing support. The Device BFM implements a complete disk store to model disk sector read/write commands. A robust set of device behaviors and error injection are provided at all protocol levels enabling realistic workload modeling.

Over 500 protocol assertion checks are built into the BFMs and link monitor to ensure the DUT complies with the specifications. A protocol assertion coverage report is generated at the conclusion of a single test or full regression. The link monitor generates several logs to codify the ATA command execution through the various protocol levels. A transaction tracker file illustrates the ATA command initiation and completion by the hosts and devices in the system. Link state tracking reports link state transitions and primitives, and a symbol tracker tracks the symbols and data on the link.

START TIME	FINISH TIME	FIS_TYPE	HOST (RX)			
			DATA			
10026297	10292697	Register_Device_to_Host	01000034	00000001	00000000	00000001
11145177	11411577	Register_Device_to_Host	01000034	00000001	00000000	00000001
12370617	12637017					
13596057	13862457	PIO_Setup	0048605f	00000001	00000000	40000001
14714937	18284697	Data	00000046	00000000	000037c8	00000000
			00000000	00000000	42424242	42424242
			41414142	41414141	00414141	00000000
			41410000	41414141	44440041	44444444

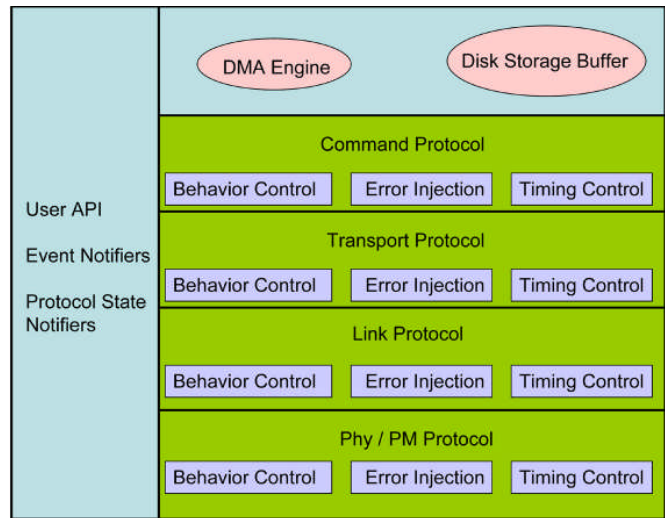
ATA transactions received by host controller

DEVICE UNDER TEST

The application designer can easily link the device under test into the test environment by instantiating the design description (RTL or gate level) into a top-level system test bench. The designer can then run the compliance suite included with the test environment and use the scenario-based test environment and BFM transaction API to create custom tests. DUT integration of the application-side logic is also supported enabling an Avery BFM to have full control over the DUT to initiate, complete, or be the target of transactions.

COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests. Tests include simple reset and sleep tests, all ATA commands, and directed tests for PIO, DMA, DMAQ, Media, CFA, Power Management, Security. Tests can be run in either PACKET and non-PACKET mode as applicable. Protocol specific functions for ATA, SATA I and II, and AHCI tests are also provided. For SATA II this includes Native Command Queuing and First Party DMA. For AHCI this includes tests for data transfer, error reporting, hot plug, power management, and platform communication. Tests are highly reusable on any design/topology based on an innovative scenarios-based methodology. Random and directed testcases are supported. Random testcases vary data and control at all CMD/TP/DLL/PHY layers and mix transaction sequences.



BFM Processing Layers and Back-End Functions

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence NC-SIM
Synopsys VCS
Model Technology ModelSim

LOCATIONS AND FACILITIES

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