

SATA-Xactor Test Environment

Your Proven Path to SATA, ATA, CE-ATA Compliance Validation

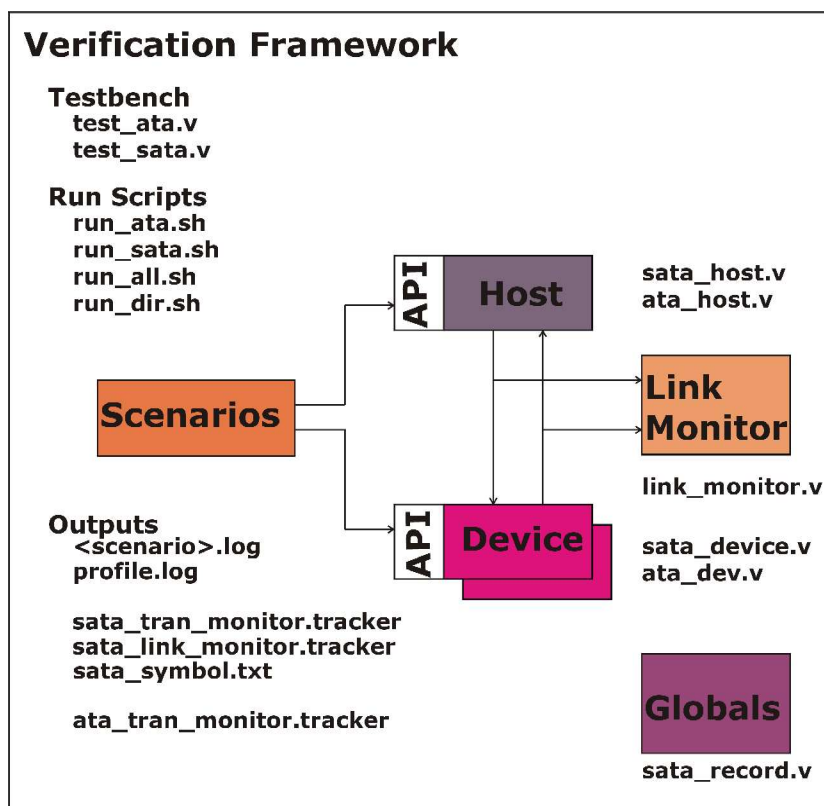


HIGHLIGHTS

- Complete solution to verify SATA I and II, ATA/ATAPI-6, CE-ATA components and peripherals
- Comprehensive BFM support – Host and Device models as Executable Reference Models (ERM)
- Comes with robust ATA/ATPA-6 and SATA Revision 2.5 compliance test suites
- Over 800 protocol checkers verify specification compliance at all layers and report violations
- Randomly mix sequence of test scenarios and parameters to create optimal test coverage under realistic conditions
- Transaction and sequential consistency is verified using design match points between DUT and shadow ERM
- Testbench frameworks ease integration of DUT and running compliance testsuites with three levels of controllability
- Supports AMBA AHB 2.0 Interface design integration
- Supports active test generation and passive link monitoring for easy integration in to any environment
- Functional coverage monitor reports device and command utilization
- Supports all environments - Verilog, SystemVerilog, Specman, Vera, SystemC, C/C++, and VHDL

OVERVIEW

The SATA-Xactor test environment is a set of behavioral models (BFMs) and test suites that simulate the behavior of the ATA, SATA, or CE-ATA components. The models, provided in Verilog model format, are tools for system designers to exercise and debug the design of components/systems based on the various ATA standards. Designs under verification (DUTs) can be verified against all realistic system topologies including host or device topologies. The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. The test environment provides a high-level test API to interact with the behavioral models supporting hosts and devices, and a link monitor which passively monitors and reports ATA, SATA, and CE-ATA protocol violations, validates end-to-end transactions, and measures and reports transaction trace analysis of devices by sector address, bytes transferred, and command types utilized. In addition, the test environment includes a full suite of compliance test scenarios that verify hosts or devices comply fully with specifications.



PROGRAMMING INTERFACE

The SATA-Xactor test environment supports a powerful transaction API for the development of diagnostic test programs and is written in native Verilog and SystemVerilog HDLs. SystemC, Specman, Vera, VHDL, and C/C++ are supported through thin-client call layers. This simple, well-defined test API enables application designers to create any combination of transaction scenarios. From a single diagnostic test program, verification engineers can control multiple BFMs, direct normal and error transactions.

VERIFICATION FRAMEWORKS

The SATA-Xactor BFMs support ATA, SATA, and CE-ATA specifications. Several complete frameworks come configured to instantiate multiple BFMs including Host, Device, and Link Monitor. DUT integration and device configuration is simplified through normal power-on and reset sequences. Compliance tests can be easily run on pre-configured testbench for rapid evaluation of DUT in the framework. Compliance tests can be reused by all of ATA and SATA host or device configurations without modifications. Protocol

checkers report assertion violations and trigger coverage. Verification test writers have the ability to selectively randomize 100s of device behaviors within the model for optimal test coverage under realistic conditions.

BFMs

The models support ATA commands including Command Register and PACKET-based execution, command queuing, and other advanced ATA command processing support. The Device BFM implements a complete disk store to model disk sector read/write commands. A robust set of device behaviors and error injection are provided at all protocol levels enabling realistic workload modeling.

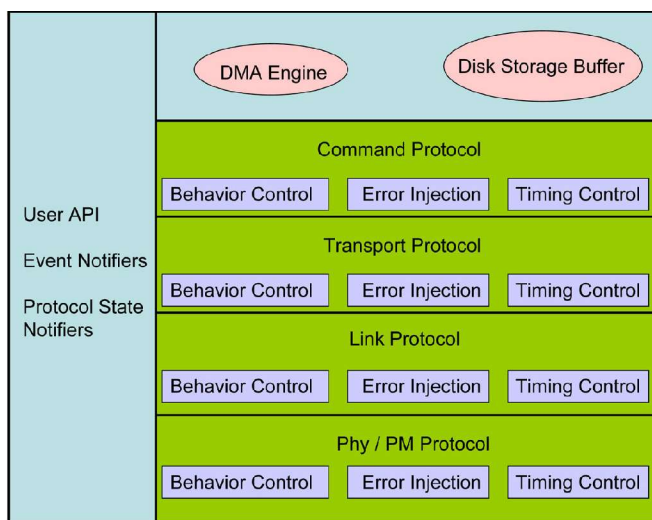
The link monitor generates several logs to codify the ATA command execution through the various protocol levels. A transaction tracker file illustrates the ATA command initiation and completion by the hosts and devices in the system. Link state tracking reports link state transitions and primitives, and a symbol tracker tracks the symbols and data on the link.

START TIME	FINISH TIME	FIS_TYPE	HOST (RX)			
			DATA			
10026297	10292697	Register_Device_to_Host	01000034	00000001	00000000	00000001
			00000000	-----	-----	-----
11145177	11411577	Register_Device_to_Host	01000034	00000001	00000000	00000001
			00000000	-----	-----	-----
12370617	12637017	-----	-----	-----	-----	-----
13596057	13862457	PIO_Setup	0048605f	00000001	00000000	40000001
			00000200	-----	-----	-----
14714937	18284697	Data	00000046	00000000	000037c8	00000000
			00000000	00000000	42424242	42424242
			41414142	41414141	00414141	00000000
			41410000	41414141	44440041	44444444

SATA transactions received by host controller

INTEGRATING DEVICE UNDER TEST

The application designer can easily link the device under test into the test environment by instantiating the design description (RTL or gate level) into a top-level system test bench. The designer can then run the compliance suite included with the test environment and use the scenario-based test environment and BFM transaction API to create custom tests. DUT integration of the application-side logic is also supported enabling an Avery BFM to have full control over the DUT to initiate, complete, or be the target of transactions. Three levels of integration are available each with more controllability to expand the compliance testing possible. DUT_0 level tests the DUT as a blackbox with just port_connect and transaction issue at the design interfaces. DUT_1 adds tasks for BFM and test scenarios to directly pass into the DUT. And DUT_2 further adds intrusiveness with inserting out of spec stimulation for testing features such as proper response to error injection. Integration of designs with AMBA AHB 2.0 interface is supported.



BFM Processing Layers and Back-End Functions

COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests. Tests include simple reset and sleep tests, all ATA commands, and directed tests for PIO, DMA, DMAQ, Media, CFA, Power Management, Security. Tests can be run in either PACKET and non-PACKET mode as applicable. Protocol specific functions for ATA, SATA I and II, and CE-ATA tests are also provided. For SATA II this includes Native Command Queuing and First Party DMA. With control using DUT integration, errors can be injected at the various protocol layers to test response of device under test. Tests are highly reusable on any design/topology based on an innovative layered scenarios-based methodology.

Random and directed testcases are supported. Random testcases vary data and control at all App/Transport/Link/PHY layers/ Avery Constrained Random Testing allows the user to easily generate thousands of highly stressful and unpredictable simulations conditions to test the DUT while checks for violations against Avery's full protocol compliance checklist items.

Random testcases vary data and control at all App/Transport/Link/PHY layers. It allows for user to randomly mix sequences of compliance test scenarios and their parameters to create optimal test coverage under realistic conditions. This expands the power of Avery's existing random-capable compliance tests to get to hard to detect design flaws..

PROTOCOL CHECKING

Over 800 protocol assertion checks are built into the BFM's and link monitor to ensure the DUT complies with the ATA/ATAPI-6 and SATA Rev 2.5 specifications. The checklist items are clearly labeled identifying the page number in the spec as well as the associated protocol layer. For example SLK.315#1 checks Link layer assertion "PHY is not ready in L_PMDeny state" on page 315 of the SATA spec. A protocol assertion coverage report is generated at the conclusion of a single test or full regression listing the checklist items that were triggered and how many times triggered as well as items that are violated.

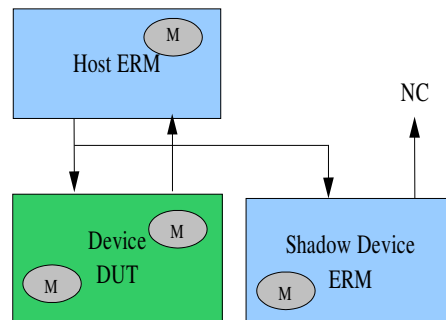
```
sata_record.sata_check_number,
sata_record.sata_profile_check_handle
("SPH.123#1": 1) = 234 : 6.92
("SPH.088#1": 2) = 11 : 0.32
("SLK.123#1": 3) = 545 : 16.11
("SPH.118#1": 4) = 32 : 0.94
("SPH.122#1": 5) = 2545 : 75.27
("SLK.159#1": 6) = 12 : 0.35
```

Protocol Checklist Report

DESIGN MATCH and AUTODEBUG

An advancement in Serial-ATA verification over traditional verification methods, Avery's SATA_Xactor coverification has an Executable Reference Model (ERM) and innovative autodebugging methods for bug detection and isolation. Using coverification the DUT and ERM run concurrently, applying the compliance and systems tests to both models. **Transaction and sequential consistency** is verified using preconfigured design match points, which track transaction flow between protocol layers of the DUT and ERM (see Figure 3). Architectural visible state and transactions are analyzed applying relaxed time, ordering, and content rules defined by the SATA protocol to ensure meaningful sequential consistency checking.

When a mismatch occurs, autodebugging is then used to perform causal analysis of the implementation model and ERM. Autodebugging utilizes enhanced behavior traversal and transaction views added to advanced behavioral debugging systems such as Novas' Verdi for better visualization of the behavior of the DUT and shadow ERM. Coverification is also especially useful in the context of random testing where expected device operation is too complex to predict or when assertions are too complex to write. Here, match points verify the architectural state of the models on-the-fly under random input sequences.



Design Match and ERM

Some example of match points include:

- End to end checking of FIS data at the Link layer from the transmitting Host to the receiving DUT Device on the other side
- Link Layer FSM State between DUT Device and Shadow (Golden) Device
- Power Management State Register between DUT Device and Shadow Device

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence
Synopsys
Model Technology

Verilog-XL NC-SIM
VCS
ModelSim

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