

PCI-Xactor Test Environment

Your Proven Path to PCI Express Compliance Validation



HIGHLIGHTS

- Complete solution for PCI Express 1.1/2.1/3.0 (Gen3), IOV, ATS, PIPE components and peripherals
- Comprehensive BFM support – Root Complex, Endpoint, Switch, PHY
- Complete testbench frameworks ease integration of DUT and running compliance testsuites
- High-level PCI transaction API supports Verilog, SystemVerilog VMM/OVM, Vera, SystemC, and VHDL
- Transaction and sequential consistency is verified using built-in reference model based scoreboard
- Directed and random compliance test suites based on PCISIG checklists and test specifications
- Comprehensive assertions track PCI-SIG compliance checklist coverage
- Functional coverage tracks range of TLP/DLLP traffic and complex operational sequences
- Packet and symbol tracker monitor output improves debug
- Models and test suites provided in SystemVerilog/Verilog source code

OVERVIEW

The PCI-Xactor test environment is a set of behavioral models (BFMs) and test suites that simulate the behavior of PCI Express devices. These complete models are written in Verilog HDL and provide the tools for system designers to exercise and debug the design of components/systems based on all PCI Express standards – PCI Express, PCI-SIG IOV, and PIPE. Designs under verification can be verified against all realistic system topologies including switch-based topologies. The objective of the models is to aid in the functional verification process prior to silicon or board fabrication. The test environment, provided in Verilog, VHDL, SystemVerilog pure, VMM, and OVM, SystemC, ANSI C/C++, and Vera, supports a high-level test API to interact with the behavioral models supporting PCI Express root complexes, endpoints, switches. A reference model scoreboard passively monitors and reports PCI Express protocol violations, validates end-to-end transactions, and measures and reports transaction trace analysis of devices by command types, power transitions, and LTSSM transitions. In addition, the test environment includes a full suite of compliance test scenarios that verify endpoint, switch, and PHY designs comply fully with the PCI Express, PCI-SIG IOV, and PIPE specifications.

Assertions

```

TXN.2.21#11  CHECKED
TXN.3.2#35  CHECKED
TXN.2.2#4   CHECKED
TXN.3.2#14  NA
...
DLL.3.1#5   CHECKED
DLL.3.1#6   NA
DLL.4.1#2   CHECKED
DLL.4.1#7   ASSERTED
PHY.2.1#2   CHECKED
CFG.10.0#1  NA
CFG.8.5#3   NA
DLL.5.2#12  CHECKED
-----
Checked items : 109 (25.41%)
Asserted items : 1 (0.23%)
    
```

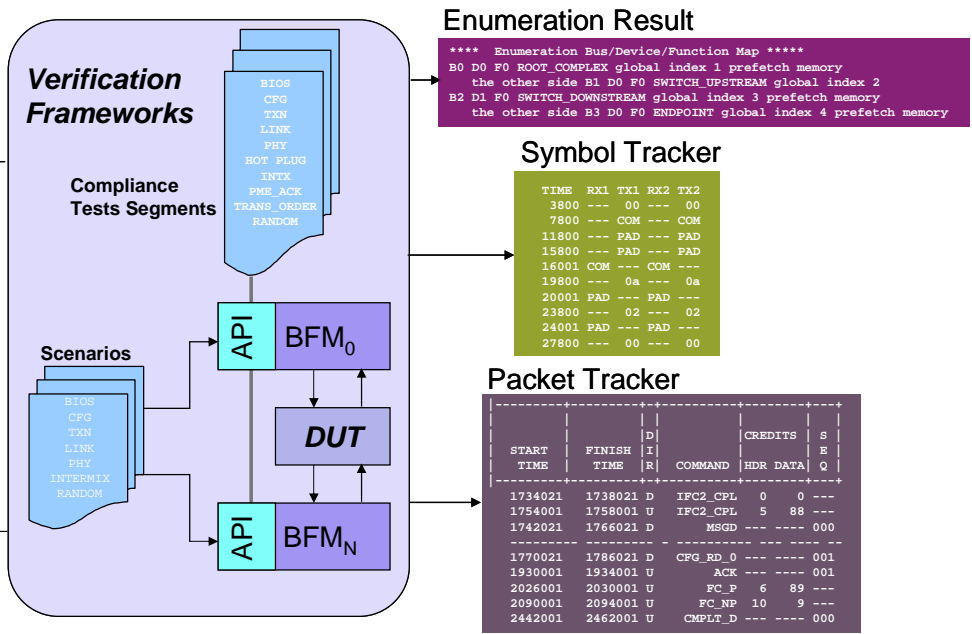
Compliance Test Coverage

```

link_test111_2port
Index  Test Name  Result
-----
1      test111rc  FAILED
2      test111ep  PASSED

link_test412_2port
Index  Test Name  Result
-----
1      test412rc  PASSED
2      test412ep  PASSED

link_test5210_2port
Index  Test Name  Result
-----
1      test5210rc  FAILED
2      test5210ep  FAILED
    
```

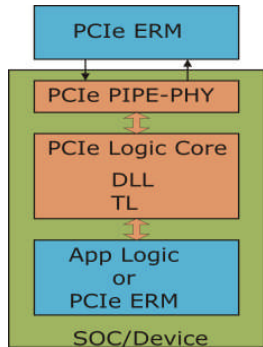


PROGRAMMING INTERFACE

The PCI-Xactor test environment supports a powerful transaction API for the development of diagnostic test programs and is written in native Verilog and SystemVerilog HDLs. Vera, VHDL, and C/C++ are supported through thin-client call layers. This simple, well-defined test API enables application designers to create any combination of PCI Express transaction scenarios. From a single diagnostic test program, verification engineers can control multiple BFMs, direct normal and error transactions, access assertions coverage, and write log files.

ENDPOINT AND SWITCH VERIFICATION FRAMEWORKS

The PCI-Xactor BFM's support PCI Express, IOV/ATS specifications. Complete endpoint, PHY, and switch frameworks come configured to instantiate multiple BFM's including PCI Express root complex, endpoint, switch, and PHY devices. DUT integration and device configuration is simplified through bios enumeration, VC negotiation, and Virtual Function discovery. Compliance tests can be reused by all configurations without modifications. Protocol checkers implement the PCISIG Checklists and report assertion violations and trigger coverage. Verification test writers have the ability to selectively randomize 100s of device behaviors (e.g., ACK/NAK response, lane-to-lane skew, etc.) within the model for optimal test coverage under realistic conditions. Each BFM contains a complete PCI configuration space with parameterized base address registers to enable easy setup of custom system simulations. Auto-enumeration of the system topology is also supported to ensure DUTs adhere to PCI system software.



SYSTEMVERILOG OVM and VMM METHODOLOGIES

PCI-Xactor supports SystemVerilog OVM and VMM methodologies fully including companion class library of environment, root complex, endpoint, switch, PHY, link monitor, and scoreboard. Built-in packet and complex operational sequence classes support constraints and coverage for robust constrained random testing. Powerful error injection and completion control using callback and built-in methods allows complex error sequences to be implemented. SystemVerilog constrained random verification stresses DUT by applying complex sequence classes modeling combinations for read/write, LTSSM transitions, L-and D-state power transitions, ACK protocol, replay, flow control, and baseline and AER error handling. A reference model-based scoreboard using an advanced DUT integration methodology verifies correct DUT vs shadow reference model behavior.

CORE THROUGH CHIP-LEVEL VERIFICATION

The PCI Express application designer can easily integrate the device under test and PCI-Xactor to form core-level or complete chip-level environments. The designer can then run the compliance suite included with PCI-Xactor or can use the transaction API to create custom tests. In core-level verification, DUT integration of the user-side logic is also supported enabling full control over the DUT to initiate transactions.

PCI EXPRESS/IOV/PIPE COMPLIANCE TEST SUITE

The test environment includes a suite of functional compliance tests based on protocol scenarios outlined in the Checklists and Test Specifications provided by the PCI Special Interest Group (PCISIG) including PCI Express root complex, endpoint, switch, and PHY. Functional compliance test coverage and assertion/checklist coverage is also provided giving a formal measure of DUT compliance. Tests are highly reusable on any design/topology based on an innovative scenarios-based methodology. Random and directed testcases are supported. Tests can be randomized at the TL/DLL/PHY layers as well at the test segment and scenario-level.

PLATFORM SUPPORT

Solaris, Linux, Windows

SIMULATOR SUPPORT

Cadence	NC-SIM
Synopsys	VCS
Model Technology	Questa

LOCATIONS AND FACILITIES

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